1. A network processor, comprising:

a crypto system;

an alignment buffer to receive header data and ciphered data from the crypto system; and

a media switch fabric having a plurality of transmit buffer elements to receive data from the alignment buffer, wherein the alignment buffer provides data to the media switch fabric in blocks having a predetermined size.

2. The network processor according to claim 1, further including an interface to transmit data from the media switch fabric.

3. The network processor according to claim 2, wherein the interface includes a SPI4 type interface.

4. The network processor according to claim 2, wherein the interface includes an NPSI interface.

5. The network processor according to claim 1, wherein the crypto system includes first and second crypto units.

6. The network processor according to claim 1, wherein the crypto system includes a predetermined number of crypto unit processing contexts and the alignment buffer includes a buffer element for each of the predetermined number of processing contexts.

7. The network processor according to claim 6, wherein the crypto system includes a plurality of cipher cores.

8. The network processor according to claim 7, wherein the plurality of cipher cores correspond to a plurality of cipher algorithms.

9. A method of processing data in a device having at least one crypto unit, comprising:

storing a portion of a packet header in an alignment buffer that has a first storage size;

storing a first portion of a first data block from the at least one crypto unit in the alignment buffer;

transmitting data from the alignment buffer to a first buffer element in a media switch fabric interface unit;

transmitting further data blocks from the alignment buffer to the first buffer element until the first buffer element is full;

allocating a second buffer element in the media switch fabric interface unit; and

transmitting data in the alignment buffer to the second buffer element.

10. The method according to claim 9, further including transmitting data from the at least one crypto unit to a selected one of a plurality of elements in the alignment buffer.

11. The method according to claim 9, wherein the alignment buffer includes a number of buffer elements corresponding to a number of processing contexts for the at least one crypto unit.

12. The method according to claim 9, further including transmitting data from the media switch fabric interface unit over an interface.

13. The method according to claim 12, further including transmitting data from the media switch fabric interface unit over an SPI4 interface.

14. The method according to claim 9, further including transmitting data from the media switch fabric interface unit over an NPSI interface.

15. The method according to claim 9, further including transmitting data from the alignment buffer in an amount that is a multiple of a predetermined number of bytes.

16. The method according to claim 15, wherein the predetermined number of bytes is 16.

17. The method according to claim 9, further including transmitting data to the second buffer element in an amount less than the predetermined number of bytes for an end of packet.

18. A network processor, comprising:

first and second crypto units each having a plurality of cipher cores and a predetermined number of processing contexts;

an alignment buffer having a respective element for each of the plurality of processing contexts to receive data from the first and second crypto units;

a media switch fabric interface unit having a plurality of transmit buffer elements to receive data from the alignment buffer in an amount that is a multiple of a predetermined number of bytes; and

an interface to transmit data from the media switch fabric.

19. The network processor according to claim 18, wherein the interface includes an SPI4 interface.

20. The network processor according to claim 18, wherein the interface includes an NPSI interface.

21. A network switching device, comprising.

a network processor including

a crypto system;

an alignment buffer to receive header data and ciphered data from the crypto system; and

a media switch fabric interface unit having a plurality of transmit buffer elements to receive data from the alignment buffer, wherein the alignment buffer provides data to the media switch fabric in blocks having a predetermined size.

22. The device according to claim 21, wherein the crypto system includes a predetermined number of crypto unit processing contexts and the alignment buffer includes a buffer for each of the predetermined number of processing contexts.

23. The device according to claim 22, wherein the crypto system includes a plurality of cipher cores.

24. The device according to claim 21, wherein the device includes a router.

25. A network, comprising.

a network switching device including a network processor having

a crypto system;

an alignment buffer to receive header data and ciphered data from the crypto system; and

a media switch fabric interface unit having a plurality of transmit buffer elements to receive data from the alignment buffer, wherein the alignment buffer provides data to the media switch fabric in blocks having a predetermined size.

26. The network according to claim 25, wherein the crypto system includes a predetermined number of crypto unit processing contexts and the alignment buffer includes a buffer for each of the predetermined number of processing contexts.

27. The network according to claim 26, wherein the crypto system includes a plurality of cipher cores.

28. The network according to claim 25, wherein the network switching device corresponds to a router.